Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DENIS DOYLE, KIERAN NUNAN and MICHAEL O'NEILL

Appeal No. 1999-0886
Application No. 08/722,738

ON BRIEF

Before KRASS, BARRETT and HECKER, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-6, all of the pending claims. Claims 7-9 were withdrawn as being directed to a nonelected invention.

The invention pertains to an electronic programmable read only memory (EPROM). An EPROM requires “hot” electrons, or “hot carrier” generation in the

channel region in order to program the EPROM. However, in the prior art, incorporation of

an EPROM cell into a standard sub-micron CMOS process, difficult because of channel lengths being less than a micron, may generate unwanted “hot” electrons in a CMOS device which would require the CMOS device to include lightly doped “hot” electron suppression regions to avoid high electric fields. However, such suppression of these “hot” electrons is undesirable for the EPROM which requires “hot carrier” generation in the channel region in order to program the EPROM.

Appellants’ solution to this dilemma is to provide an EPROM having a field effect transistor (FET) connected to a capacitor. Relatively heavy doped regions are selectively formed in the EPROM FET and are inhibited from being formed in the CMOS transistors. These heavily doped regions dominate the EPROM FET lightly doped “hot” electron suppression regions to enable programming of the EPROM. As summarized by appellants in the brief, the device is a memory which has a charge storing capacitor coupled to the gate electrode and adapted to store charge produced in the channel region in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode. In order to store

charge in the capacitor, hot carriers must be generated during programming for storage in the capacitor.

Representative independent claim 1 is reproduced as follows:

1. A electronic programmable read-only-memory comprising:

(a) a field effect transistor having: relatively heavy doped source and drain regions separated by an oppositely doped channel region; a gate electrode disposed over the channel region; lightly doped regions, having the same conductivity type as the source and drain regions, extending laterally from the source and drain regions to peripheral regions of the channel region; and, relatively heavy doped regions, having the same conductivity type as the source and drain regions, extending laterally from the source and drain regions, through and beyond the lightly doped regions, into the channel region; and

(b) a charge storing capacitor coupled to the gate electrode and adapted to store charge produced in the channel region in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode.

The examiner relies on the following references:

Nakamura et al. (Nakamura)	5,300,799	Apr. 05, 1994
Hamamoto et al. (Hamamoto)	5,146,300	Sep. 08, 1992
Miller et al. (Miller)	5,046,043	Sep. 03, 1991
Momi	JP 06-132,489	May 13, 1994

Claims 1-6 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner offers Nakamura and Momi with regard to claims 1, 2, 4 and 5, adding Hamamoto and Miller to the combination with regard to claims 3 and 6.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

In rejecting claims 1 and 4, the examiner identifies Nakamura as disclosing an EPROM with FETs Tr1-Tr8, having source/drain regions 5 and capacitors FC1-FC8 coupled to gates 8. The examiner recognizes that Nakamura does not disclose the LDD structure of the instant claimed invention but relies on Figures 1 and 8 and the abstract of Momi for the suggestion to use an LDD structure, including a source and drain region, lightly doped regions, heavily doped regions, gate electrode and a channel region, to eliminate the injection of hot electrons into the gate oxide and stop soft leak. The examiner then concludes that it would have been obvious to incorporate the LDD structure of Momi into Nakamura's device "to eliminate the injection of hot electrons into the gate oxide and stop soft leak" [answer-page 3].

Appellants contend that Nakamura stores information using the polarization of the ferroelectric capacitor and does not store charge generated in the channel region in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode. Contrary to Nakamura, the instant claimed

device does include a charge storing capacitor coupled to the gate electrode adapted to store charge produced in the channel region in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode.

Appellants further note that the Momi abstract and Figures suggest a transistor configured to "stop soft leak," or to suppress the generation of carriers in the channel region which get transferred through the gate oxide to the gate conductor. Accordingly, contend appellants, the skilled artisan would not use a carrier *suppression* transistor, as taught by Momi, in the device of appellants' claimed invention which *relies* on the generation of channel carriers which get transferred to the capacitor in order to program the device [reply brief-page 2].

The examiner's response [answer-page 4] is merely to state that "[i]f the claimed invention and the structurally similar prior art species share a useful property, that will generally be sufficient to motivate an artisan of ordinary skill to make the claimed species." However, the examiner fails to elucidate as to what he means by this. Moreover, the examiner contends that it is "well known" to "adapt ferroelectric capacitors to store charge in semiconductor memories since such materials can store 100 times the charge of a typical dielectric...of the same thickness" and that, therefore,

it would have been obvious to adapt the gate-coupled capacitor of Nakamura "to store charge because of the superior charge storing properties of ferroelectric material" [answer-page 4]. However, the examiner has provided no suggestion, other than appellants' own disclosure, for adapting Nakamura's gate-coupled capacitor to store charge in the manner claimed. Merely because the capacitor of Nakamura *can be* so adapted is not a reason, within the meaning of 35 U.S.C. § 103, for doing so. There must be some reason, suggested by the prior art or by the knowledge of artisans, for adapting the capacitor of Nakamura to store charge produced in the channel region in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode. The examiner has not convinced us of such a reason.

Additionally, the examiner answers appellants' comments regarding the "teaching away" aspects of Momi by merely stating that it would have been obvious to "incorporate the LDD structure as taught by Momi into the device of Nakamura...to stop soft leak" [answer-page 5]. This is an insufficient response to appellants' reasonable argument that Momi's soft leak stoppage *suppresses* the generation of carriers in the channel region and that the skilled artisan would not use a carrier *suppression*

transistor, as taught by Momi, in the device of appellants' claimed invention which *relies* on the generation of channel carriers which get transferred to the capacitor in order to program the device.

Appellants argue that Nakamura discloses a capacitor which "is a ferroelectric storage non-volatile memory device by itself. It stores either a logic one or a logic 0 in accordance with the polarity of a programming voltage applied across the electrodes of the capacitor" [reply brief-page 3]. As pointed out by appellants, Nakamura discloses, at column 1, lines 9-10, that the device stores information using a residual dielectric polarization of a ferroelectric substance. It is not, like the instant claimed invention, a device which is programmed by transferring charge to it.

The examiner employs Momi merely for its disclosure of an LDD structure and its elimination of injection of hot electrons into the gate oxide to stop soft leak. Thus, the examiner has provided no evidence, by either of the applied references, of the capacitor of the instant claimed invention which is "adapted to store charge produced in the channel region in response to a logic state programming voltage applied between one of the source and drain regions and the gate electrode."

We hold that the examiner has not presented a prima facie case of obviousness with regard to the instant claimed subject matter and, to whatever extent that such a

prima facie case may be said to have been made, appellants have presented convincing arguments to overcome any such case.

Accordingly, the examiner's decision rejecting claims 1-6 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS)
Administrative Patent Judge)
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LEE E. BARRETT) APPEALS AND
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